

## CLAIMS

1        1. A method for preventing passive release of interrupts within a computer system, the computer system having at least one processor for servicing the interrupts, one or  
2        more input/output (I/O) devices configured to issue interrupts, and an I/O bridge having a  
3        plurality of ports to which I/O devices are coupled and configured to interface between  
4        the I/O devices and the processor, the method comprising the steps of:  
5

6                asserting an interrupt signal by a subject I/O device coupled to a given port of the  
7        I/O bridge;

8                forwarding an interrupt message corresponding to the interrupt signal to the processor for servicing;

9                setting an interrupt pending flag in response to assertion of the interrupt signal;

10                in response to the interrupt being serviced, generating a first ordered message, the  
11        first ordered message notifying the subject I/O device that the interrupt has been serviced;

12                generating a second ordered message for clearing the interrupt pending flag;

13                sending the first ordered message to the given port of the I/O bridge;

14                sending the second ordered message to the given port of the I/O bridge after the  
15        first message has been sent;

16                deasserting the interrupt signal in response to the first message; and

17                clearing the interrupt pending flag at the interrupt file in response to the second  
18        ordered message.

1        2. The method of claim 1 further comprising the step of forwarding the first ordered message from the given I/O bridge port to the subject I/O device.

1        3. The method of claim 2 wherein the step of deasserting the interrupt signal is  
2        performed by the subject I/O device following its receipt of the first ordered message.

1        4. The method of claim 3 wherein the I/O bridge further includes an interrupt port  
2        and the interrupt pending flag is disposed at the interrupt port, the method further com-

3 prising the step of forwarding the second ordered message from the given I/O bridge port  
4 to the interrupt port.

1 5. The method of claim 4 wherein  
2 the interrupt pending flag is implemented through a register of the interrupt port;  
3 and  
4 the second ordered message is a write transaction to the register for clearing the  
5 interrupt pending flag.

1 6. The method of claim 5 further comprising the steps of:  
2 periodically collecting a set of information regarding the assertion of interrupt  
3 signals by I/O devices; and  
4 after the step of clearing the interrupt pending flag, waiting a predetermined time  
5 before collecting a next set of information regarding the assertion of interrupt signals.

1 7. The method of claim 6 wherein the step of periodically collecting is performed  
2 through one or more serial data transfer operations.

1 8. The method of claim 1 wherein the steps of generating the first and second or-  
2 dered messages are performed by the processor.

1 9. The method of claim 8 wherein the computer system includes (1) a plurality of  
2 processors at least one of which is designated to service interrupts from the subject I/O  
3 device, and (2) a plurality of I/O bridges each I/O bridge coupled to a plurality of I/O de-  
4 vices configured to assert respective interrupt signals.

1 10. The method of claim 1 wherein the interrupt signals are level sensitive inter-  
2 rupts (LSIs).

1 11. A computer system comprising:

2 a plurality of input/output (I/O) devices configured to assert and deassert respec-  
3 tive interrupt signals;

4 at least one processor for servicing interrupts from the I/O devices; and  
5 an I/O bridge configured to interface between the I/O devices and the at least one  
6 processor, the I/O bridge having a plurality of ports to which the I/O devices are coupled  
7 and an interrupt controller configured to detect the assertion and deassertion of the inter-  
8 rupt signals, wherein

9 the interrupt controller, in response to assertion of an interrupt signal by a subject  
10 I/O device coupled to a given I/O bridge port, issues an interrupt message to the proces-  
11 sor and sets an interrupt pending flag;

12 the processor, upon servicing the interrupt, sends first and second ordered mes-  
13 sages to the given port of the I/O bridge, the first ordered message notifying the subject  
14 I/O device that the interrupt has been serviced, and the second ordered message clearing  
15 the interrupt pending flag;

16 the subject I/O device deasserts the interrupt signal in response to the first mes-  
17 sage; and

18 the interrupt pending flag is cleared in response to the second ordered message.

1 *13.* The computer system of claim 12 wherein

2 the I/O bridge further includes an interrupt port at which the interrupt controller is  
3 disposed, and

4 the given port of the I/O bridge forwards the second ordered message to the inter-  
5 rupt port after forwarding the first ordered message to the subject I/O device.

1 *14.* The computer system of claim 13 wherein the interrupt port of the I/O bridge  
2 includes at least one register at which the interrupt pending flag is implemented.

1 *15.* The computer system of claim 12 wherein

2 the I/O bridge port includes a read cache for buffering messages received from the  
3 at least one processor, and an ordering engine operatively coupled to a read cache, and

4           the ordering engine is configured to release ordered messages buffered in the read  
5    cache in the same order as which they were received.

1           16. The computer system of claim 12 further comprising an interrupt collector  
2    having a parallel-load shift register for receiving the interrupt signals from the I/O de-  
3    vices, the serial shift register configured to transfer information indicating the assertion or  
4    deassertion of interrupt signals to the interrupt controller through one or more serial shift  
5    operations.

1           17. The computer system of claim 16 wherein  
2           the interrupt collector transfers the information in response to a request from the  
3    interrupt controller, and  
4           the interrupt controller is configured to limit the number of serial shift operations  
5    performed by the interrupt collector so as to receive only information associated with in-  
6    terrupt signals that have been enabled.

1           18. The computer system of claim 12 wherein the interrupt signals are level sen-  
2    sitive interrupts (LSIs).

F O T O S O C I E T Y